UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,194 B2
DATED : August 30, 2005
INVENTOR(S) : Jacques Prunier

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Lines 46-47, should read -- each mulitiplexer Mi is connected to the input Di of same rank. A first input terminal of each multiplexer Mi is connected to --.
Line 66, should read -- TD3, TD2, and TD1 are successively presented to terminal SI at the --.

Column 3,
Line 1, should read -- circuit operation. When the circuit is tested, signal TEST is --.

Column 4,
Line 22, should read -- before sequentially reading the data contained in the register. --.
Line 55, should read -- elements bearing the same references in Fig. 3, connected in --.

Column 5,
Line 55, should read -- do not include an error that maintains signal EN1 active. --.

Column 6,
Line 23, should read -- test register. Vector TD6, TD5, and TD4 is chosen to give the --.
Line 42, should read -- and FF1 and provided to input terminals I3, I2, and I1 from time t3 --.

Column 7,
Line 42, should read -- readily occur to those skilled in the art. Disturbing elements --.
Line 44, should read -- There are many types of elements disturbing the scan test, --.

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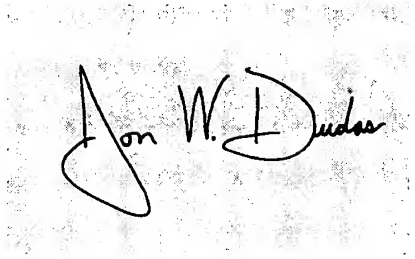
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8,
Line 2, should read -- a single logic block and three flip-flops, but --.

Signed and Sealed this

Eighth Day of November, 2005



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